What Is Claimed Is:

1. A input/output buffer protection circuit, comprising:

an I/O pad;

an I/O buffer, comprising a first PMOS transistor and a first NMOS transistor;

an n-well control circuit coupled to an n-well of the first PMOS transistor and the I/O pad for raising the n-well of the first PMOS transistor to a input voltage level when the input voltage is greater than a source voltage;

a gate control circuit coupled to a gate terminal of the first PMOS transistor and the n-well control circuit for raising the gate terminal of the PMOS transistor to the input voltage level when the input voltage is greater than the source voltage, the gate control circuit comprises a transistor for passing a control voltage to the gate of the PMOS transistor in output mode; and

wherein the n-well control circuit comprising a protection component, providing a voltage drop down path from the gate of the transistor to the I/O pad and block the I/O pad signal flow back to the gate of the transistor.

2. The input/output buffer protection circuit of claim 1, wherein the N-Well control circuit comprising:

a second PMOS transistor, wherein the gate terminal of the second PMOS is connected to a source voltage V_{CC}, a

source terminal of the second PMOS is connected to the I/O pad, and the drain terminal of the second PMOS is connected to the n-well of the PMOS transistor of the I/O buffer;and

a third PMOS transistor, wherein the gate terminal of the third PMOS is connected to a source voltage, a source terminal of the third PMOS is coupled to the I/O pad, a n-well of the third PMOS is connected to the drain terminal of the second PMOS; and

a fourth PMOS transistor, wherein the gate terminal of the fourth PMOS transistor is connected to the drain of the third PMOS, a source terminal is connected to the source voltage, and the drain terminal of the fourth PMOS is connected to the n-well of the third PMOS.

3 The input/output buffer protection circuit of claim 2, wherein the transistor of the gate control circuit is a sixth PMOS transistor, the gate control circuit further comprising:

a fifth PMOS transistor,

wherein the gate terminal of the fifth PMOS is connected to the source voltage, the source terminal is connected to the I/O pad ;

a sixth PMOS transistor, wherein the gate terminal is connected to the drain of the third PMOS, a source terminal is connected to the control signal, and a drain terminal coupled to the gate of the first PMOS; and

a second NMOS transistor, wherein a gate terminal of the NMOS is connected to the source voltage, a drain terminal is connected to the control signal, and a

source terminal is connected to the gate of the first PMOS.

4. The input/output buffer protection circuit of claim 1 or claim 3, wherein the protection component is an NMOS transistor.

5. The input/output buffer protection circuit of claim 4, wherein a gate terminal and a source terminal are coupled to a node A which is connected to the gate of the sixth PMOS transistor, a drain terminal of the NMOS transistor is connected to the I/O pad.

6. The input/output buffer protection circuit of claim 1, wherein the protection component is a PMOS transistor.

7. The input/output buffer protection circuit of claim 1, wherein the protection component is a diode configured device.